REMARKS

Claims 30-32, 34, 35 and 59 have been amended. Claims 29-32, 34-39, 41, 44-47, 49 and 51-64 are currently pending in this application. Applicant reserves the right to pursue the original and other claims in this and other applications. Applicant respectfully requests reconsideration of the application in light of the following remarks.

Applicant gratefully acknowledges the indication of allowable subject matter in claims 29-32 and 34-35.

Claims 55-58 and 60-64 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Agarwal et al. (U.S. Patent No. 6,297,527) ("Agarwal") in view of Aoki et al. (U.S. Patent No. 6,033,953) ("Aoki"). This rejection is respectfully traversed and reconsideration is respectfully requested.

Claim 55 recites a container capacitor including a "lower electrode provided within a first insulating layer, said lower electrode comprising an electropolished patterned metal layer having a bottom wall and vertical sidewalls extending rectangularly upwardly therefrom," a "second insulating layer provided over said electropolished patterned metal layer and in contact with said first insulating layer," and an "upper electrode provided over said second insulating layer."

Claim 60 recites a container capacitor structure including an "insulating layer provided over a substrate," a "plurality of rectangular openings provided in said insulating layer," a "plurality of lower capacitor electrodes provided along the bottom and sidewalls of respective ones of said rectangular openings, said lower electrodes being formed as discrete electropolished metal layers," and a "dielectric layer

associated with each of said discrete lower electrodes, said dielectric layer being in contact with said insulating layer."

Both of claims 55 and 60 require that the insulating layer provided over the metal layer is "in contact with the [first] insulating layer." The Office Action states that Agarwal discloses this structural feature. (Office Action, pg. 2-3). Applicant respectfully disagrees. Agarwal's dielectric layer 72, which arguably corresponds to the second insulating/dielectric layer of the claims, is not in contact with the protective layer 64, which arguably corresponds to the first insulating layer of the claims.

Aoki is relied upon as disclosing using an electropolishing method. (Office Action, pg. 3-4). Aoki does not disclose, teach or suggest a "second insulating layer provided over said electropolished patterned metal layer and in contact with said first insulating layer" as recited in claim 55 or a "dielectric layer being in contact with said insulating layer" as recited in claim 60. Further, Aoki relates to a process of electropolishing an already patterned metal layer. Even if Agarwal and Aoki were properly combinable, which Applicant does not concede, the combination does not disclose, teach or suggest all of the limitations of claims 55 and 60.

Accordingly, claims 55 and 60 are allowable over the cited combination. Claims 56-58 depend from claim 55 and are allowable along with claim 55. Claims 61-64 depend from claim 60 and are allowable along with claim 60. Applicant respectfully requests that the rejection of claims 55-58 and 60-64 be withdrawn and the claims allowed.

Claims 36-39, 41, 44-47, 49, 51-54 and 59 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Agarwal in view of Aoki and further in view of

Huang (U.S. Patent 6,127,260) ("Huang"). This rejection is respectfully traversed and reconsideration is respectfully requested.

Claim 36 recites a memory cell including a "transistor including a gate fabricated on a semiconductor substrate and including a source/drain region in said semiconductor substrate disposed adjacent to said gate," an "electropolished patterned metal layer within an insulating layer provided over said substrate, said electropolished patterned metal layer having a thickness of about 50 to about 300 Angstroms," and a "container capacitor including a lower electrode, a dielectric layer over said lower electrode, and an upper electrode over said dielectric layer, said upper electrode comprising doped polysilicon, said lower electrode having a surface aligned over said source/drain region, said electropolished patterned metal layer forming said lower electrode, and said dielectric layer being in contact with said insulating layer."

Claim 44 recites a processor-based system including a processor and an integrated circuit coupled to said processor. At least one of the integrated circuit and processor includes a "container capacitor provided within an insulating layer, said container capacitor including a lower electrode and an upper electrode, said lower electrode comprising an electropolished patterned metal layer having a thickness of approximately 50 to 300 Angstroms, wherein a top surface of said electropolished patterned metal layer is at the same level with a top surface of said insulating layer, said upper electrode comprising doped polysilicon."

Claim 59 recites a container capacitor including an "insulating layer provided over a substrate, said insulating layer containing an opening," a "tantalum nitride barrier conductive layer provided at a bottom of said opening," a "lower electrode provided over said tantalum nitride barrier conductive layer, said lower electrode comprising an electropolished patterned metal layer having a bottom and vertical

sidewalls extending upwardly from said bottom, said lower electrode having a thickness of approximately 100 Angstroms," a "dielectric material provided over said electropolished patterned metal layer and in contact with said insulating layer," and an "upper electrode comprising doped polysilicon provided over said dielectric material and wherein said lower electrode, said dielectric material and said upper electrode form a container capacitor."

With respect to claims 36 and 59, Agarwal does not disclose, teach or suggest the "dielectric layer being in contact with the insulating layer," for at least the reasons previously discussed with respect to claims 55 and 60. Aoki is relied upon as disclosing using an electropolishing method (Office Action, pg. 5), and as previously discussed, does not disclose, teach or suggest a "dielectric layer being in contact with said insulating layer" as recited in claim 36. Huang is relied upon as disclosing an upper electrode comprising doped polysilicon. (Office Action, pg. 5). The Office Action points to the upper plate structure 35 of Huang for disclosing this limitation. (Office Action, pg. 5). Applicant respectfully disagrees. Huang discloses the storage node contact structure 32 as being formed of doped polysilicon, but does not disclose, teach or suggest the upper plate structure 35 comprising doped polysilicon. (Huang, col. 5, lines 30-59). Huang also does not disclose, teach or suggest the "dielectric layer being in contact with the insulating layer."

With respect to claim 44, Agarwal does not disclose, teach or suggest "a top surface of the metal layer is at the same level with a top surface of the insulating layer." Agarwal's metal layer is at least partially located above the top surface of the insulating layer and therefore, the top surface of the metal layer cannot be at the same level with a top surface of the insulating layer. (Agarwal, Figures 1-8). Aoki is relied upon as disclosing using an electropolishing method. (Office Action, pg. 6). As previously discussed, Aoki relates to a process of electropolishing an already patterned metal

layer. Aoki also does not disclose, teach or suggest "a top surface of the metal layer is at the same level with a top surface of the insulating layer." Huang is relied upon as disclosing an upper electrode comprising doped polysilicon. (Office Action, pg. 6). For at least the reasons discussed above, Applicant respectfully disagrees that Huang discloses this limitation. Huang also does not disclose, teach or suggest "a top surface of the metal layer is at the same level with a top surface of the insulating layer."

Accordingly, claims 36, 44 and 59 are allowable over the cited combination. Claims 37-39 and 41 depend from claim 36 and are allowable along with claim 36. Claims 45-47, 49 and 51-54 depend from claim 44 and are allowable along with claim 44. Applicant respectfully requests the rejection of claims 36-39, 41, 44-47, 49, 51-54 and 59 be withdrawn and the claims allowed.

In view of the above amendment, Applicant believes the pending application is in condition for allowance.

Dated: October 13, 2006

Respectfully submitted,

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